IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1-30. (Canceled)

- 31. (Previously Presented) A semiconductor capacitor storage poly, comprising: downwardly extending recesses; and a plurality of contiguous mesas comprising a plurality of contiguous top surfaces forming a maze-like structure.
- 32. (Previously Presented) The storage poly of claim 31, wherein the mesas extend in the X, Y and Z coordinates.
- 33. (Previously Presented) A semiconductor capacitor storage poly, comprising:
 downwardly extending recesses;
 a plurality of contiguous webs comprising a plurality of contiguous top surfaces forming a mazelike structure; and
 hemispherical-grain polysilicon on at least some of the plurality of contiguous top surfaces.
- 34. (Previously Presented) The storage poly of claim 33, wherein the webs extend in the X, Y and Z coordinates.
- 35. (Previously Presented) An intermediate semiconductor capacitor structure,
 comprising:
 a storage poly structure comprising a plurality of contiguous mesas with recesses therebetween;
 a contiguous hemispherical-grain polysilicon layer on the storage poly structure and in contact therewith;
 and

- a mask over the hemispherical-grain polysilicon layer, the recesses being exposed through the contiguous hemispherical-grain polysilicon layer and the mask.
 - 36. (Canceled)
- 37. (Previously Presented) An intermediate semiconductor memory cell structure, comprising:
- a storage poly structure;
- a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer on the storage poly structure;
- recesses formed in the storage poly structure and located laterally between the plurality of contiguous low elevation regions of the hemispherical-grain polysilicon layer; and dielectric material at least lining the recesses.
- 38. (Previously Presented) A semiconductor memory cell structure, comprising: a storage poly structure;
- regions of hemispherical-grain polysilicon on at least portions of an upper surface of the storage poly structure;
- a plurality of recesses extending into the storage poly structure, at least some recesses of the plurality of recesses being located laterally between the regions of hemispherical-grain polysilicon and imparting the storage poly structure with a structure resembling a plurality of contiguous mesas; and
- and a dielectric layer substantially coating an upper surface of the storage poly structure and substantially lining each of the plurality of recesses.
- 39. (Previously Presented) The semiconductor memory cell structure of claim 38, further comprising a cell poly structure over the dielectric layer.

- 40. (Previously Presented) The semiconductor memory cell structure of claim 38, wherein the regions of hemispherical-grain polysilicon have a web-like appearance.
- 41. (Previously Presented) The semiconductor memory cell structure of claim 38, wherein at least some of the plurality of recesses extend into the storage poly structure.
- 42. (Previously Presented) An intermediate semiconductor capacitor structure, comprising:
- a storage poly structure;
- a substantially confluent hemispherical-grain polysilicon layer on the storage poly structure; and a mask positioned over the substantially confluent hemispherical-grain polysilicon layer, planarized portions of the hemispherical-grain polysilicon layer being exposed through the mask.
- 43. (Previously Presented) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure including recesses therein;

remaining portions of a hemispherical-grain polysilicon layer having a web-like appearance and substantially overlying upper portions of the storage poly structure; and

- a mask positioned over the hemispherical-grain polysilicon layer, laterally between the recesses, and substantially spaced apart from the storage poly structure by the remaining portions of the hemispherical-grain polysilicon layer, the recesses in the storage poly structure being exposed through the mask.
- 44. (Previously Presented) An intermediate semiconductor capacitor structure, comprising:
- a storage poly structure with recesses therein;
- a hemispherical-grain polysilicon layer having a web-like appearance on at least portions of the storage poly structure; and

dielectric material lining at least the recesses.

45. (Previously Presented) An intermediate semiconductor memory cell structure, comprising:

a storage poly structure with recesses therein;

low elevation regions of a hemispherical-grain polysilicon layer having a web-like appearance on at least portions of the storage poly structure; and dielectric material at least lining the recesses.